TABLE II
COMPARISON ON THE DESIGN OF THE IMPEDANCE TRANSFORMER BY THE IDEAL INVERTOR MODEL AND THE GENERALIZED INVERTOR MODEL

		Ideal design		Generalized design	
0		0.8595mm		0.8595mm.	
1		2.0790mm		2.0798mm	
2		5.6937mm		5.7006mm	
3		9.9254mm		9.9254mm	
L_1	θ_1	5.5676mm	0.2500π	5.6673mm	0.2545π
L_2	θ_2	5.5676mm	0.2500π	5.5676mm	0.2527π

Comparison of the ideal design and the generalized design for the impedance transformer is shown in Table II. The response curves of the two transformers are simulated and plotted in Fig. 6, where the ideal design (using the ideal invertor model) is unable to deal with the discontinuity of the step and thus evades it [3]. On the contrary, the generalized design (using the generalized model) copes with the discontinuity easily. The design comparison shows the formulae given by the generalized model is more accurate than the ideal one as discontinuities are considered.

IV. CONCLUSION

The new model of the generalized invertor is proposed for the symmetric- and asymmetric-type. It is suitable to general circuits networks instead of fewer lumped circuits. The new model is apt to be applied to the design of the passive network directly.

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A Design Procedure for Monolithic Matrix Amplifier

Claudio Paoloni and Stefano D'Agostino

***Abstract*—A procedure for the design of monolithic matrix amplifier is proposed. A simplified expression for small signal gain based on unilateral field-effect transistor (FET) model is derived. In particular, the Design-Oriented FET model previously published is adopted. The introduction of a set of design charts allows the designer a fast and accurate prediction of low frequency gain and 3-dB cutoff frequency of a given matrix amplifier. Good agreement with experimental data and simulations confirms the validity of the proposed design method.**

I. INTRODUCTION

Matrix amplifier, due to the combination of multiplicative and additive amplification principle, represents a suitable solution when very wide frequency band and high gain are required. Many realizations have been recently presented in the literature [1]–[3].

Theoretical studies on matrix amplifier were also published [4]. Unfortunately, the complexity of the mathematical formulations limits their applicability to practical design. This becomes especially true when the parasitics of the field-effect transistor (FET) composing the amplifier are included in the computation. Approximate expressions for small signal gain were given, but partially, help to solve the problem.

In this paper a simple formula to accurately predict the matrix amplifier frequency response will be proposed. The formula in conjunction with the Design-Oriented FET model reported in [5] provides an effective and accurate prediction of matrix amplifier performance. As it was demonstrated, the Design-Oriented FET model effectively takes into account the FET parasitics, maintaining at the same time the simplicity of the unilateral model.

A straightforward process-independent graphical design procedure for matrix amplifier is also defined to provide the designer a fast

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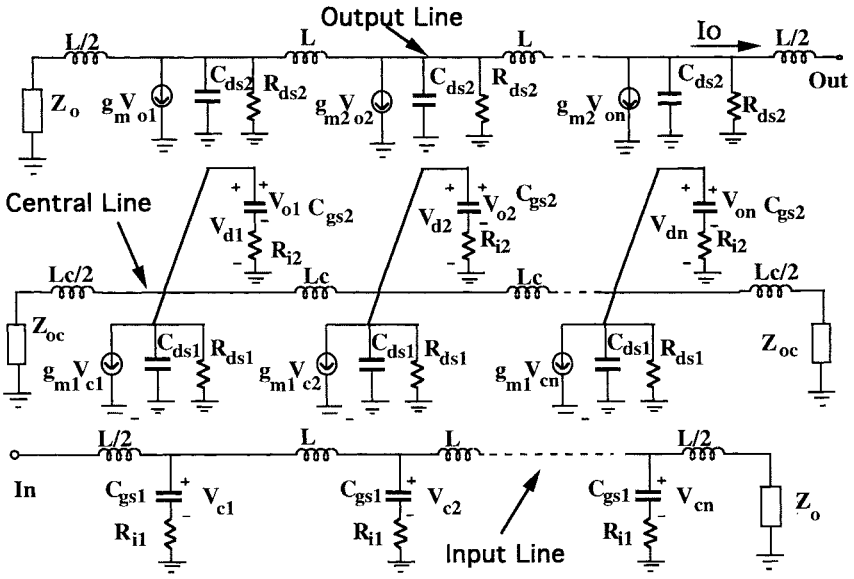


Fig. 1. Schematic of matrix amplifier.

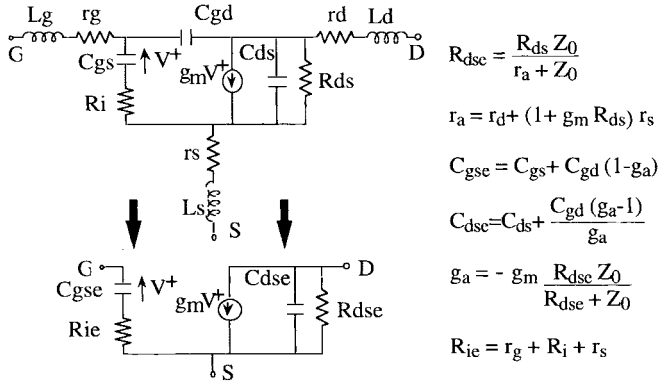


Fig. 2. Design-oriented FET model.

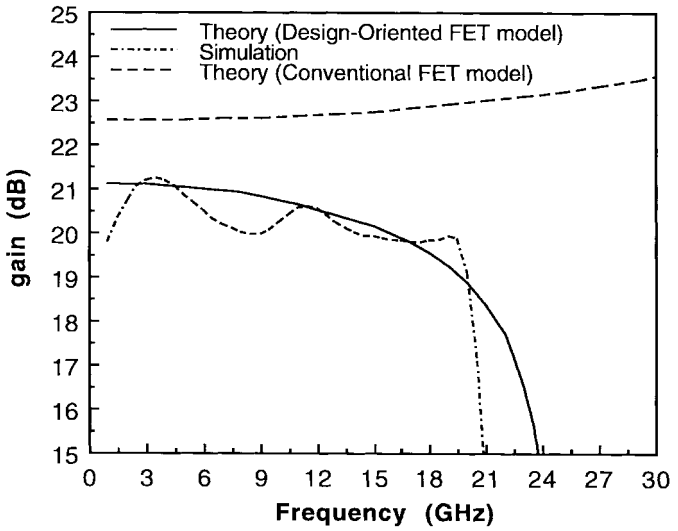


Fig. 3. Comparison between theory and simulation for a 2×4 matrix amplifier.

and accurate design tool. The validity of the proposed theory will be demonstrated by comparison with simulations and experimental results from the literature.

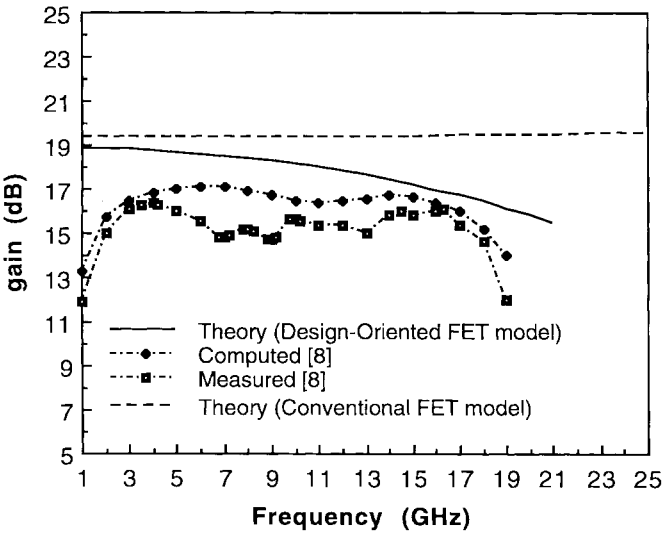


Fig. 4. Comparison between theory and data from [8].

II. Theory

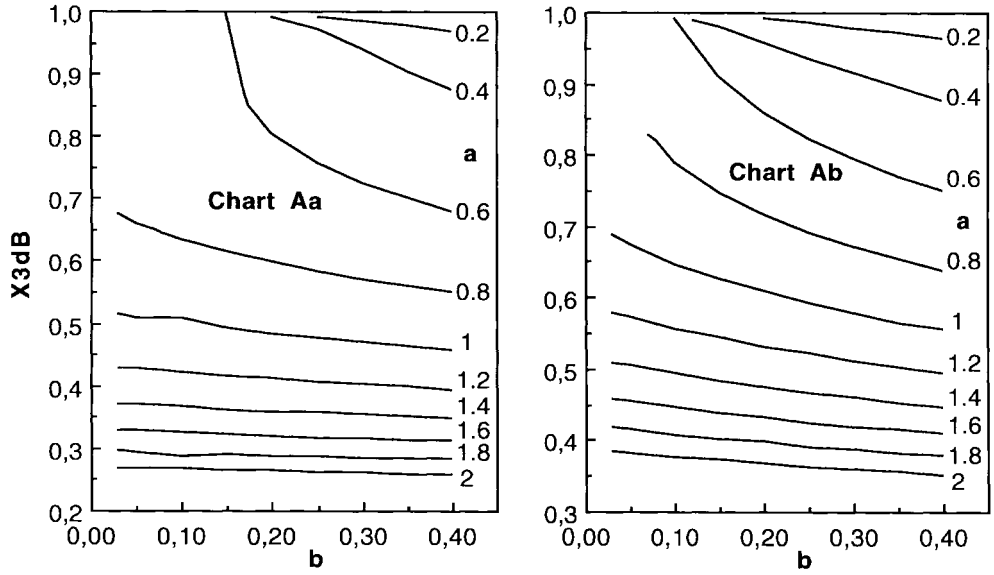
The matrix amplifier, assuming a unilateral FET model approximation, can be schematized as in Fig. 1. The two-tier matrix amplifier will be considered in the following, since represents the common case of MIC [4], [6] and MMIC [1]–[3], [7], [8] realizations.

Three artificial transmission lines can be individuated in the circuit: input line, central line, and output line. Assuming the distributed amplification principle [9], the three transmission lines are imposed to have the same cutoff frequency and consequently the same phase velocity. Typically the cutoff frequency f_c of the input and the output transmission line is

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{\pi\sqrt{LC_{\rm gs1}}} = \frac{1}{\pi\sqrt{L(C_{\rm ds2} + C_{\rm add})}} \tag{1}$$

and the characteristic impedance is

$$Z_0 = \sqrt{\frac{L}{C_{\rm gs1}}} = \sqrt{\frac{L}{C_{\rm ds2} + C_{\rm add}}} = 50\ \Omega. \tag{2}$$



(a) (b)

Fig. 5. Fractional bandwidth $X_{3\,\mathrm{dB}}$ as a function of the term b for different term a [Chart Aa ($N = 2$); Chart Ab ($N > 2$)].

Particular attention must be devoted to the central line where the shunt capacitance is equal to $C_{\mathrm{gs}2} + C_{\mathrm{ds}1}$. To impose the phase velocity of the central line equal to the phase velocity of the input and the output transmission line, the series inductance must be recalculated as

$$L_c = \frac{1}{\pi^2 f_c^2 (C_{\mathrm{gs}2} + C_{\mathrm{ds}1})} \tag{3}$$

and consequently the characteristic impedance of the central line Z_{0c} results

$$Z_{0c} = \sqrt{\frac{L_c}{C_{\mathrm{gs}2} + C_{\mathrm{ds}1}}}. \tag{4}$$

The analytical procedure applied to distributed amplifier in [9] will be extended to matrix amplifier topology. The Design-Oriented FET model [5] (Fig. 2) is adopted in the computation to include, in a simple manner, the FET parasitics (in the following: $C_{\mathrm{gs}} = C_{\mathrm{gse}}$; $C_{\mathrm{ds}} = C_{\mathrm{dse}}$; $R_i = R_{ie}$; $R_{\mathrm{ds}} = R_{\mathrm{dse}}$).

The output current I_0 can be expressed as

$$I_0 = \frac{1}{2} g_{m2} e^{-\frac{\Theta_{d2}}{2}} \sum_{k=1}^{N} V_{dk} \frac{e^{-\tan^{-1}\left(\frac{\omega}{\omega_{g2}}\right)}}{\sqrt{1 + \left(\frac{\omega}{\omega_{g2}}\right)^2}} e^{-(n-k)\Theta_{d2}} \tag{5}$$

where

- g_{m2} transconductance of the FET's on the second row;
- ω_{g2} $1/R_{i2}C_{\mathrm{gs}2}$;
- N number of FET's in the amplifier;
- V_{dk} voltage applied to the gate of the k-th FET of the second row;
- Θ_{d2} propagation constant of the output line.

The voltage V_{dk} is approximated, without affecting significantly the accurateness of the formulation, assuming a "zero-frequency" hypothesis, as

$$V_{dk} = \frac{N Z_{0c} R_{\mathrm{ds}1}}{N Z_{0c} + 2 R_{\mathrm{ds}1}} g_{m1} V_{ck} \tag{6}$$

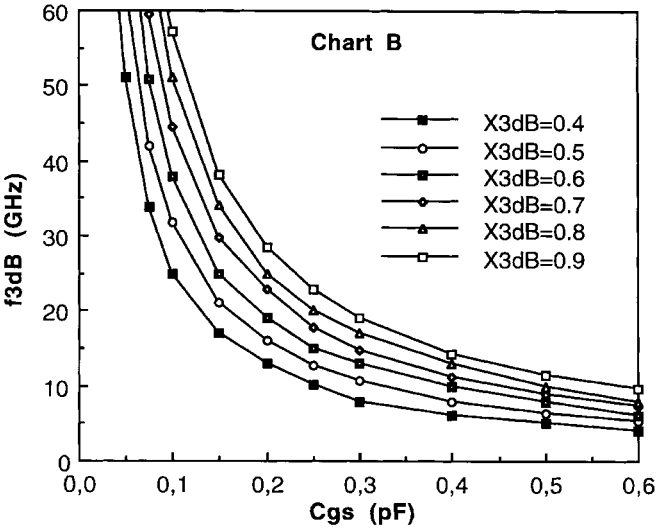


Fig. 6. Chart B: 3-dB cutoff frequency $f_{3\,\mathrm{dB}}$ versus the FET gate-source capacitance C_{gs} for different fractional bandwidth $X_{3\,\mathrm{dB}}$ values.

where

- g_{m1} and $R_{\mathrm{ds}1}$ transconductance and the output resistor of the FET's on the first row, respectively;
- V_{ck} voltage applied to the C_{gs} of the kth FET on the first row.

Assuming the same analytical steps adopted in [9] the small signal gain can be expressed as (7), shown at the bottom of the page, where

- A_{d2} attenuation of the output line [9];
- A_{g1} attenuation of the input line [9];
- ω_{g1} $1/R_{i1}C_{\mathrm{gs}1}$.

$$A_\omega = \frac{1}{2} g_{m1} g_{m2} Z_0 \frac{N Z_{0c} R_{\mathrm{ds}1}}{N Z_{0c} + 2 R_{\mathrm{ds}1}} \frac{e^{-\frac{N}{2}(A_{d2} + A_{g1})} \sinh\left(\frac{N}{2}(A_{d2} - A_{g1})\right)}{\sqrt{1 + \left(\frac{\omega}{\omega_{g1}}\right)^2} \sqrt{1 + \left(\frac{\omega}{\omega_{g2}}\right)^2} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \sinh\left(\frac{A_{d2} - A_{g1}}{2}\right)} \tag{7}$$

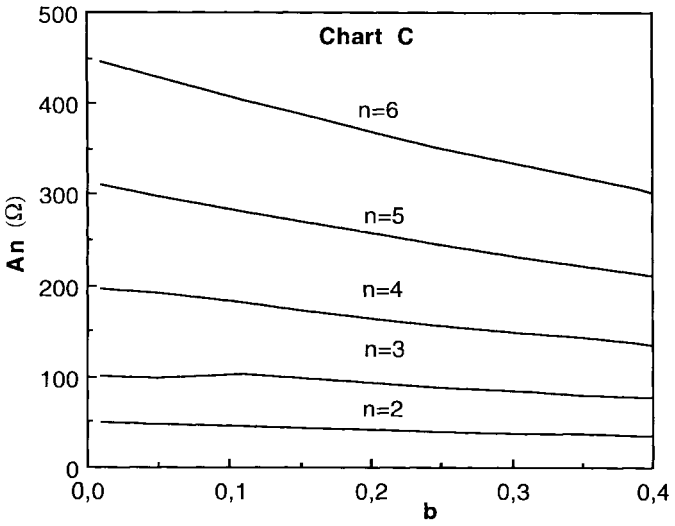


Fig. 7. Chart C: Term A_n as a function of the term b and number of FET's N.

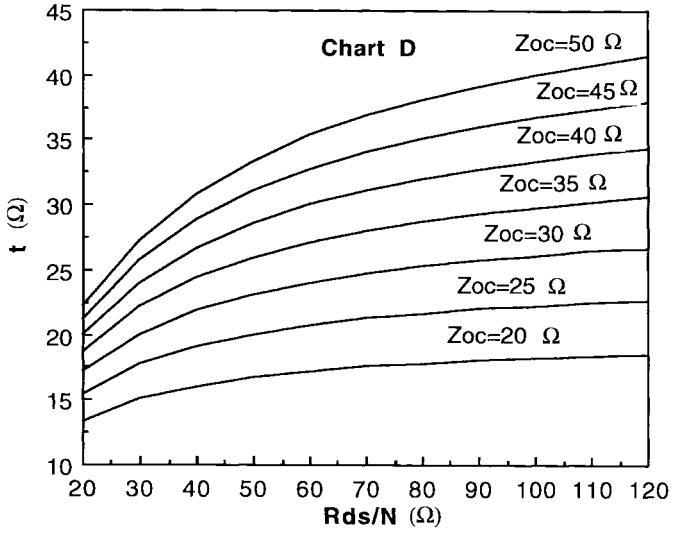


Fig. 8. Chart D: Term t as a function of $R_{\rm ds}/N$ for different values of Z_{0c}.

Expression (7) can be rearranged, as is shown in [9], introducing the terms $a = N\frac{R_i}{Z_0}$ and $b = \frac{N}{4}(\frac{Z_0}{R_{\rm ds}})$, so as the low-frequency gain A_0 can be expressed as

$$A_0 = \frac{1}{2} g_{m1} g_{m2} N Z_0 \frac{Z_{0c} R_{\rm ds1}}{N Z_{0c} + 2R_{\rm ds1}} \frac{\sinh(b) e^{-b}}{\sinh(b/N)}. \tag{8}$$

To prove the validity of the presented theory to predict small signal gain for matrix amplifier, comparisons with simulated and measured results will be presented. Remarks on the importance of using the Design-Oriented FET Model for the accurateness of the result will also be presented.

In Fig. 3 the small signal gain of a 2×4 matrix amplifier designed using AlGaAs HEMT reported in [10] is shown. The simulated gain of the circuit (performed by Libra$^{(TM)}$) is compared with the results obtained from (7) computed adopting both the conventional unilateral FET model and the Design-Oriented FET model. A comparison of theoretical results with measured and simulated data for the 2×4 matrix amplifier published by Chang *et al.* [8] is presented in Fig. 4.

Both examples clearly show a satisfactory agreement of this theory with data obtained from measurements and circuit simulations by using CAD packages. The effectiveness of the simple formula presented, in the prediction of matrix amplifier small signal gain, is therefore confirmed. The use of the Design-Oriented FET model is mandatory to include the effects of the FET parasitics.

III. Design Procedure

The formulation expressed by (7) can be effectively used to define a design procedure, independent from active device, to predict, in term of 3-dB cutoff frequency $f_{3\,\rm dB}$ and low frequency gain A_0, matrix amplifier performance for a given FET and the number of FET's per row N.

The fractional bandwidth is defined as [5]

$$X_{3\,\rm dB} = \frac{f_{3\,\rm dB}}{f_c} \tag{9}$$

where $f_{3\,\rm dB}$ is the 3-dB cutoff frequency of matrix amplifier expressed as

$$f_{3\,\rm dB} = \frac{X_{3\,\rm dB}}{\pi C_{\rm gs} Z_0}. \tag{10}$$

The low-frequency gain A_0 (8) can be rewritten as

$$A_0 = g_{m1} g_{m2} A_n t \tag{11}$$

where

$$A_n = \frac{Z_0}{4} N \frac{\sinh(b) e^{-b}}{\sinh(b/N)} \tag{12}$$

$$t = \frac{Z_{0c} R_{\rm ds}/N}{Z_{0c}/2 + R_{\rm ds}/N}. \tag{13}$$

After these assumptions four design charts were derived from (7) and (11).

Chart A (Fig. 5, Aa for $N = 2$, Ab for $N > 2$) plots the fractional frequency $X_{3\,\rm dB}$ behavior as function of term b for different values of term a. Chart B (Fig. 6) plots the 3-dB cutoff frequency $f_{3\,\rm dB}$ versus the FET gate-source capacitance $C_{\rm gs}$ for different fractional bandwidth $X_{3\,\rm dB}$ values.

The term A_n is plotted in Chart C (Fig. 7) as a function of the b term (for $N = 2, 3, 4, 5, 6$). Chart D (Fig. 8) provides the term t as a function of the central line characteristic impedance Z_{0c} and of the ratio $R_{\rm ds}/N$.

The simple design procedure to predict the frequency response of matrix amplifier can be outlined as follows.

First, the Design-Oriented FET model is calculated for the FET chosen to design the matrix amplifier and the terms a and b are then computed.

The 3-dB cutoff frequency $f_{3\,\rm dB}$ for the considered matrix amplifier is obtained from Chart B as a function of $C_{\rm gs}$ and the $X_{3\,\rm dB}$ value previously derived from Chart A. The term A_n is derived from Chart C for the given number of FET's N and the corresponding term b. The term t is obtained from Chart D assuming the Z_{0c} value calculated from (4). Finally the low-frequency gain A_0 is obtained substituting the values of A_n and t in (11).

The generalized nature of simple procedure described allows a fast prediction of the performance of matrix amplifier, maintaining the accuracy demonstrated for (7).

IV. Conclusion

A new and simple formula to predict the frequency behavior of matrix amplifier is presented. This formula in conjunction with the Design-Oriented FET model, previously presented, allows good accuracy and fast implementation. A graphical design procedure has been defined to provide a useful tool to designers for fast prediction of matrix amplifier performance. The comparison with experimental and simulated data demonstrates the effectiveness of this simple method.

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Calculation of Distributed Capacitances of Spiral Resonators

Zunfu Jiang, P. S. Excell, and Z. M. Hejazi

***Abstract*— A method for calculating the distributed capacitances and resonant frequencies of spiral resonators is described. First, the charge distribution on a spiral is found by a simplified model and the moment method, then the distributed capacitance is calculated. The equivalent inductance of the spiral resonator is then evaluated according to a standard formula, and the resonant frequencies are finally computed. The calculated results are compared with experimental data, and a good agreement between them is shown.**

I. INTRODUCTION

Planar spirals have certain advantages as electrically small resonators, but their characteristics are not well understood and empirical design methods tend to be used. Experimental results for some characteristics of planar spiral resonators are described in [1]. The equivalent circuit of a planar spiral resonator can be made up of an inductance, a capacitance, and a resistance. The inductances of thin-film planar spirals are considered in [2]–[4]. An empirical formula, with limited accuracy, for calculating the distributed capacitance of planar spirals is given in [5] as

$$C = 0.035 D_o + 0.06 \quad [\text{pF}] \tag{1}$$

where D_o is the outer diameter of the spiral in millimeters. This formula is only approximate as it clearly neglects several relevant parameters.

The inductance and resistance of a planar spiral resonator can be computed with sufficient accuracy from the available literature. While the resonant frequencies of spiral inductors can also be predicted using standard software packages, there is a high cost in computational time and it is useful to have analytical expressions if they can be found. For this, a simple effective method for the capacitance is the main need.

In this paper, a method for calculating distributed capacitances and resonant frequencies of spiral resonators is described. First, the charge distributions on the spirals are found by a simplified model and the moment method. Then, the distributed capacitances of the spiral resonators are calculated. The equivalent inductances of the spiral resonators are then evaluated according to a standard formula and the resonant frequencies are finally computed and compared with experimental data from Nishi *et al*. [1].

II. CALCULATION OF THE DISTRIBUTED CAPACITANCE

A planar spiral resonator system includes a spiral on a substrate, coupling circuits, and a shield box. For simplicity, a spiral in a uniform dielectric medium with permittivity ε is considered and is illustrated, with an equivalent circuit, in Fig. 1.

It is assumed that the capacitance C_o per unit length of the spiral resonator is given (see Section III). Following the method described in [8], the total distributed capacitance C of the spiral resonator can be

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